Synopsis V1.0
Proton SEE test of Virtex4 FPGA XC4VFX60 from Xilinx

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I. Introduction

This study has been undertaken to determine the single event effect susceptibility of the Xilinx Virtex 4 Field Programmable Gate Array (FPGA) XC4VFX60. Device under test (DUT) was monitored for destructive events induced by exposing it to a proton beam at the Indiana University Cyclotron Facility (IUCF). Test was performed in the frame of HST/RNS project.

II. Devices Tested

Device part number is XC4VFX60-10FF1152CES1. Device technology is 90 nm Copper CMOS from UMC. Device is packaged in a 1152 pin flip-chip fine pitch BGA package. We used parts from HST/RNS flight lot. Part marking is shown in Table 1.

Table 1: test samples package marking

Xilinx VIRTEX-4 XC4VFX60 FF1152DGQ0609 DD1394545A 11I-ES1	Xilinx Virtex-4 XC4VFX60 FF1152DGQ0609 DD1401594A 11I-ES1

III. Test Facility

Facility: Indiana University Cyclotron Test Facility (IUCF)
Beam: 52, 89, 200 MeV protons
Flux: 4×10^6 to 4×10^8 particles/cm^2/s.
Fluence: all tests were run to 1×10^{11} p/cm^2 or until destructive or functional events occurred.

IV. Test Conditions and Error Modes

Test Temperature: ~60˚C (die)*
Operating Frequency: 250 MHz for Power PC, 62 MHz for I/Os
Power Supply Voltage: Vccint: 1.2V
Vccaux**:** 2.5V
Vcco: 3.3V

* maximum junction temperature is 125˚C. Die temperature is given by DUT internal temperature sensing diode.

PARAMETERS OF INTEREST: Power supply currents, device functionality

SEE Conditions: SEL, SEU, MEU, SET, SEFI

V. Test Set-up

XC4VFX60 was tested with NASA-GSFC REAG (Radiation Effects and Analysis Group) high-speed digital tester (HSDT). HSDT is a reusable universal digital device tester based on Xilinx Virtex 2 Pro FPGA with input/output (I/O) operation speed up to 600 MHz.

High-speed tester is the main test board that interfaces with the DUT-specific daughter card. The DUT on the daughter card is exercised using the configurable FPGA on high-speed tester with Hardware Design Language such as VHDL based coding. A remote PC controls the tester. XC4VFX60 daughter board includes 2 banks of 2Mx16 bit SRAM (one bank for each power PC), and one 22Mbit flash PROM to store DUT configuration. In addition, via the JTAG interface, DUT can be configured, and configuration memory can be read back. Figure 1 shows the general test-set-up during irradiation. More details about test set-up can be found in [1]

Figure 2 shows a picture of the high-speed tester with XC4VFX60 daughter board in front of proton beam line at IUCF. We tried to shield as much as possible HSDT board as well as SRAMs mounted on daughter board from particles. HSDT Virtex2-pro FPGA and memories are sensitive to proton-induced SEUs. Cypress SRAMs on DUT daughter board are sensitive to proton-induced SEUs and micro-latchups[2].

[1] Heavy ion SEE test of Vitex-4 XC4VFX60 from Xilinx, test report, June, 2007
[2] Proton SEL test of Virtex-4 FPGA XC4VFX60 from Xilinx, test report, February 2007

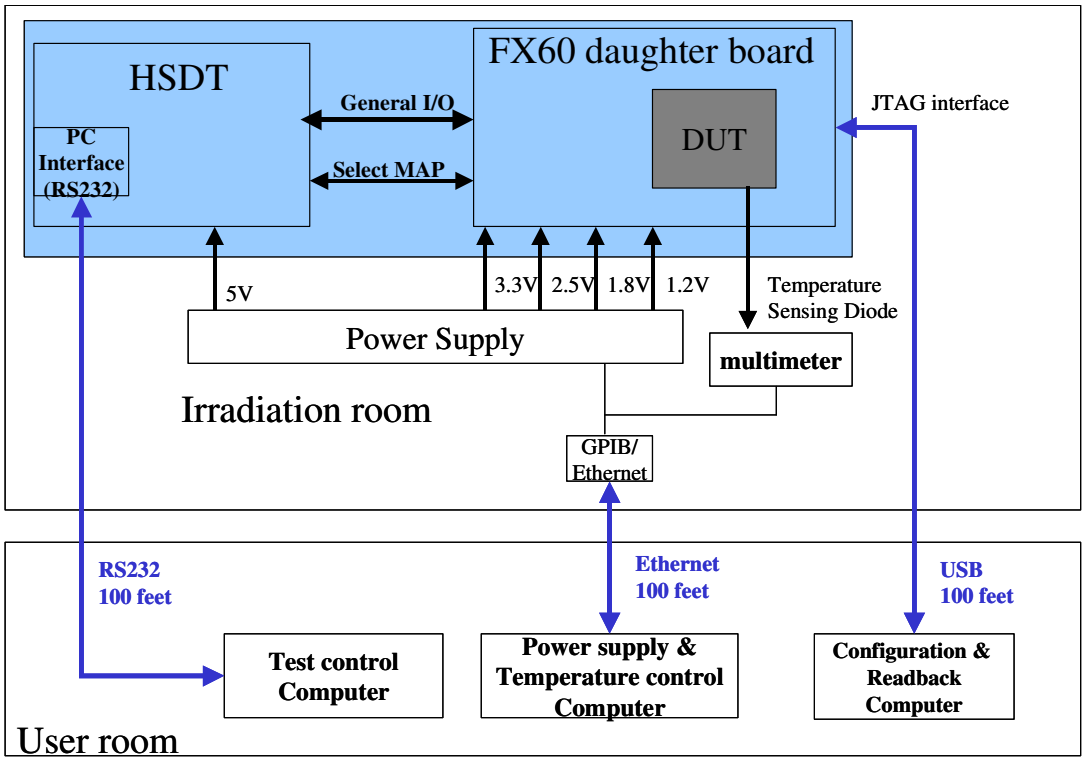

Figure 1: XC4VFX60 test set-up

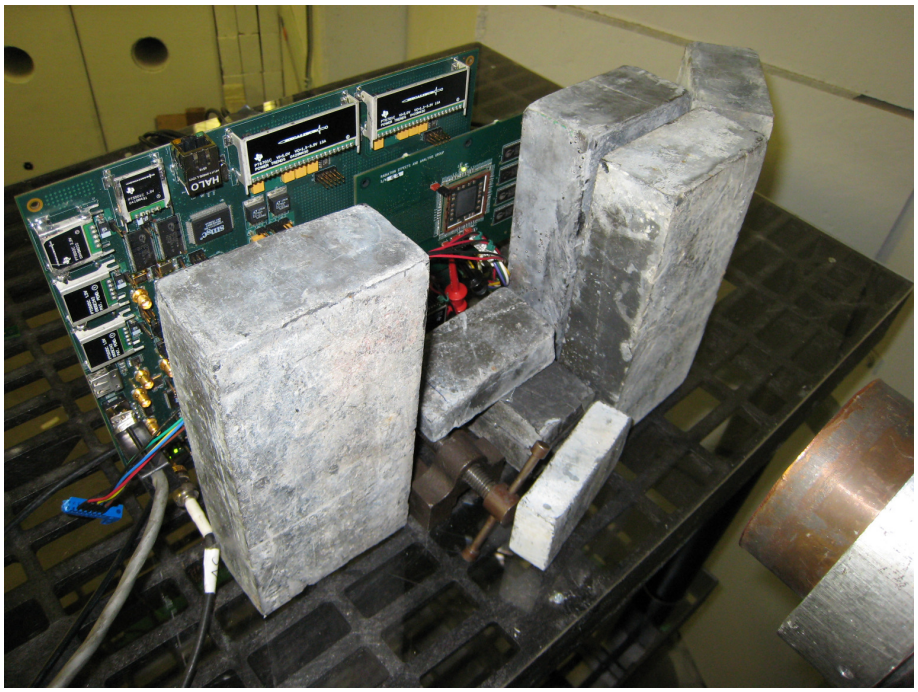

Figure 2: high-speed tester with XC4VFX60 daughter board in front of proton beam line at IUCF

DUT design is basically made of the two XC4VFX60 embedded power PCs and one large shift register. The Power PC section of the DUT consists of two identical circuits each centered around one of the embedded power PC 405 processors. The tester feeds a single clock signal at a frequency of 62.5 MHz to the DUT. The processor runs at a frequency of 250 MHz generated by a local Digital Clock Manager (DCM). Each processor circuit contains a Processor Local Bus (PLB) that is the main memory bus of the processor and runs at 62.5 MHz. Each Power PC interfaces with one of the 2Mx16 SRAM banks on the DUT daughter board. External SRAMs on daughter board house both the instruction memory and data memory for all operations of the power PCs.

Each processor communicates to the tester board either through a UART that is attached to an On chip Peripheral Bus (OPB) connected to the PLB by a PLB to OPB bridge or through a high speed parallel port. Via this port the tester board can access directly the external SRAMs banks through a multiplexer within the DUT.

One version of the design includes the Xilinx self-scrubbing of configuration memory with on chip Internal Configuration Access Port (ICAP).

Separately from the power PC circuits, 8 x 2000 flip-flop shift registers are implemented. Each shift register runs at 125 Mhz with a 4-bit parallel output operating at 31.25 Mhz representing the next 4 bits of the shift register. These shift registers are presented to the tester board as a 32-bit word with an associated 31.25 Mhz shift_clock.

Two different test programs have been used:

- Multi interrupt or “ping-pong” program: Each PPC simply waits for a critical or non-critical interrupt. Then, when the interrupt is received, a counter is incremented corresponding to the types of interrupt that is received and a message is sent out through the UART or high speed parallel port to HSDT board.
- One critical interrupt program: Tester sends a critical interrupt to each processor. This starts a principal counting program.

During irradiation, DUT power supply currents (Vccint (1.2V), Vccaux(2.5V), and Vcco(3.3V)) were monitored. Nominal DUT power supply currents are 440 mA, 70 mA, and 95 mA for Vccint, Vccaux, and Vcc0 respectively. As soon as one of the current reaches a programmable SEL detection level (750 mA for core, 500 mA for aux, 1 A for I/O), the DUT power supplies were shutdown and irradiation was stopped.

DUT die temperature was measured via the DUT internal temperature sensing diode. Power supply and temperature monitoring and control are performed with a Labview program running on a laptop.

Another Labview program running on another laptop interfaced with HSDT. It set test modes and collected telemetry. HSDT program performed two tasks during the irradiation. Shift register was exercised but not tested:

- Scrub of DUT configuration memory: all configuration memory but BRAM is scrubbed at a frequency of 31 MHz, scrubbing command is a manual command from Labview program. Test can be run with and without scrubbing. The time between scrubs is programmable. This scrub is a blind scrub that does not rely on readback and analysis of

readback frame CRC as scrubbing can be done by other teams. DUT configuration is stored in HSDT SRAM and each configuration 32- bit word is rewritten every 15 ms.

- Test of the two power PCs in DUT. With the multi-interrupt test program, the HSDT program sends regularly (time between interrupts is programmable) interrupt requests (critical and non critical) to each power PC, collects the processor response to interrupt requests and sends the messages to the Labview program. If one of the Power PC hangs (no response to interrupt request), a timeout signal is sent to the Labview program. With the "one critical interrupt" program, HSDT program sends one critical interrupt to each power PC, then it collects the data from the processor. When data stop coming, a timeout signal is sent to the Labview program. Test start is a manual command from Labview program.

More details about HSDT test commands are given in [1].

Test procedure is a follows. In case of an event (time out or SEL) irradiation is stopped, and the following sequence is applied:

- reset PPC and restart PPC (manual Labview commands)

If DUT is up and running again, another irradiation run can be started. If it does not work:

- Reset DUT and restart DUT (manual Labview commands)

If DUT is up and running again, another irradiation run can be started. If it does not work:

- Unconfigure and reconfigure DUT (manual Labview commands)

If DUT is up and running again, another irradiation run can be started. If it does not work:

- Reload test programs in SRAMs

If DUT is up and running again, another irradiation run can be started. If it does not work:

- Power cycle DUT and reconfigure

If DUT is up and running again, another irradiation run can be started. If it does not work:

- Resend DUT configuration bit file to the tester and reconfigure DUT

If DUT is up and running again, another irradiation run can be started. If it does not work:

- Power cycle tester board and DUT, reconfigure tester and DUT

If DUT is up and running again, another irradiation run can be started

After each irradiation run, content of DUT configuration memory was readback with Xilinx IMPACT software tool. IMPACT allows configuration, readback of configuration memory, and readback with verify though JTAG interface. IMPACT does the verification of configuration memory with a CRC code.

VI. Test Results

All tests were performed with the high-speed port. Even though proton beam was collimated and SRAMs were shielded (see Figure 2), 3 microlatchup in SRAMs were observed. The 3 irradiation runs with microlatchup were ignored in the analysis. Table 2 shows a summary of test results obtained with multi-interrupt program.

Table 2: average measured cross-sections for all parts and all runs

SN #	Scrub	IT (ms)	Cache	Energy (MeV)	Tilt (°)	Flux (#/cm^2-s)	Fluence (#/cm^2)	SEFI #	X SEFI (cm^2/dev)	CL max (cm^2/dev)	CL min (cm^2/dev)	Comments
S3	self (ICAP)	100	no	91	0	4.78E+07	2.09E+10	2	9.57E-11	3.01E-10	1.70E-11	
S3	self (ICAP)	100	no	202	0	6.44E+07	6.97E+09	4	5.74E-10	1.31E-09	1.96E-10	
S3	self (ICAP)	100	no	200	0	5.35E+06	6.88E+09	4	5.82E-10	1.33E-09	1.99E-10	
S3	self (ICAP)	100	no	200	0		1.38E+10	8	5.78E-10	1.04E-09	2.88E-10	average
S3	self (ICAP)	100	no	200	45	5.02E+07	1.24E+10	4	3.23E-10	7.38E-10	1.10E-10	
S3	no	100	no	52.3	0	1.60E+07	1.49E+10	3	2.01E-10	5.21E-10	5.49E-11	
S3	no	100	no	88.9	0	4.71E+07	1.65E+10	2	1.21E-10	3.82E-10	2.16E-11	
S3	no	100	no	200	0	3.48E+07	6.13E+09	7	1.14E-09	2.14E-09	5.36E-10	
S3	no	100	no	200	45	6.43E+07	4.69E+09	4	8.53E-10	1.95E-09	2.91E-10	
S8	no	100	no	200	0	1.32E+08	3.52E+09	3	8.52E-10	2.20E-09	2.32E-10	
S3	no	100	yes	200	0	1.47E+07	3.05E+09	5	1.64E-09	3.44E-09	6.46E-10	
S3	no	1	no	200	0	1.36E+07	3.93E+09	5	1.27E-09	2.68E-09	5.02E-10	
	no	100	no	200	0		8.21E+09	7	8.53E-10	1.60E-09	4.00E-10	average
S3	no	1000	no	200	0	1.75E+07	3.21E+09	5	1.56E-09	3.27E-09	6.13E-10	
S3	external	100	no	93	0	4.91E+07	3.66E+10	1	2.73E-11	1.29E-10	1.40E-12	
S3	external	100	no	204	0	6.56E+07	3.08E+10	3	9.75E-11	2.52E-10	2.66E-11	
S3	external	100	no	200	45	5.07E+07	1.42E+10	5	3.53E-10	7.43E-10	1.39E-10	
S8	external	100	no	200	0	5.16E+07	1.20E+10	1	8.35E-11	3.96E-10	4.28E-12	
S3	external	100	no	200	0	1.42E+07	2.17E+10	3	1.38E-10	3.58E-10	3.77E-11	
S3	external	100	no	200	0	1.12E+08	2.64E+10	3	1.14E-10	2.94E-10	3.10E-11	
S3	external	1	no	200	0	8.90E+07	6.08E+09	5	8.23E-10	1.73E-09	3.24E-10	
	external	100	no	200	0		9.08E+10	10	1.10E-10	1.87E-10	5.98E-11	average
S3	external	1000	no	200	0	6.86E+07	4.82E+10	3	6.23E-11	1.61E-10	1.70E-11	

Figure 3 shows SEFI cross-sections versus interval time between interrupt requests. We can see that without scrubbing SEFI cross-sections do not change with interval time between interrupt requests. This is an indication that without scrubbing SEFI are mostly caused by errors in FPGA fabric (routing errors due to upsets in configuration memory), and therefore, the way the PPC is tested does not make any difference. To the contrary, with scrubbing, SEFI cross-section increases significantly, about one order of magnitude, when interval time between interrupt requests decreases from 1s to 1 ms.

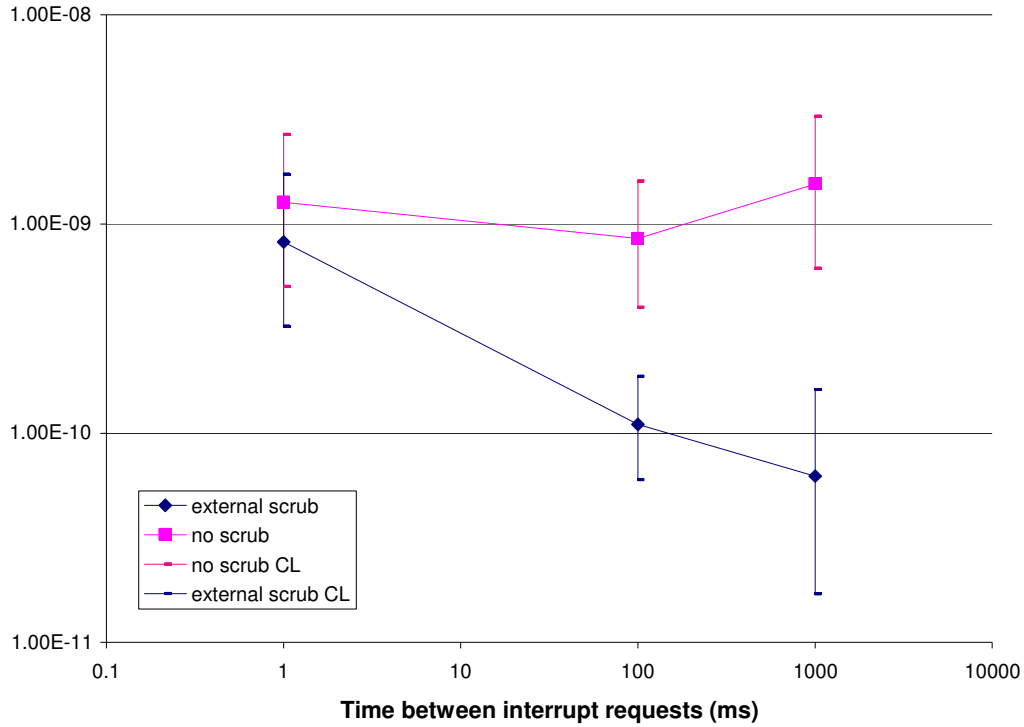

Figure 3: SEFI cross-sections versus interval time between interrupt requests

Figure 4 shows SEFI cross-section versus energy for a time interval between interrupt requests of 100 ms. As observed during heavy ion testing, we can see that external scrubbing provides a significant improvement with a reduction of SEFI cross-sections by about one order of magnitude. Self-scrub provides little improvement at 89 MeV and factor 2 improvement at 200 MeV.

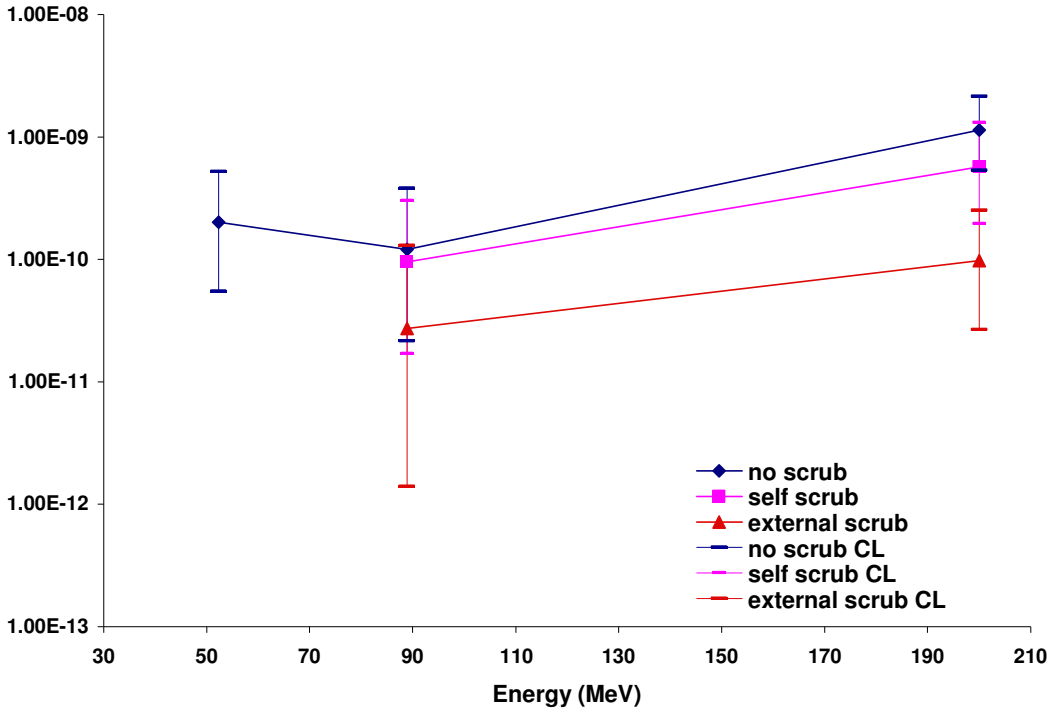

Figure 4: SEFI cross-sections versus energy for an interval time of 100 ms between interrupt requests

On one occurence a power cycle was necessary to recover from SEFI. However, because of hits in USB interface and SRAM storing configuration memory, it is difficult tell what happened. When JTAG interface was not working we power cycled DUT at first. Then, we tried to just unplug USB cable from the computer and plug again. By doing that we restored JTAG interface and we were able to make a readback at the end of irradiation runs. This did not work one time only. During reconfigurations we had to send bit files as we often had a handful of errors in SRAM storing configuration memory.

In most cases we had to reconfigure DUT. Figure 5 shows that almost 100% of SEFI needed a reconfiguration to recover from when DUT configuration memory was not scrubbed. Without scrubbing FPGA is going down before the PPCs.

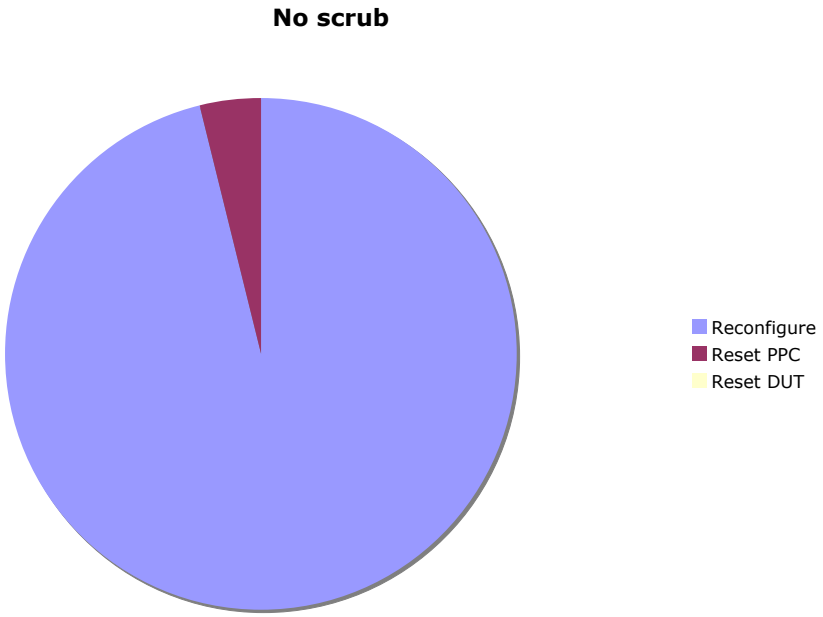

Figure 5: recoveries from SEFI when DUT configuration memory is not scrubbed

Figure 6 shows the SEFI recovery modes when DUT was self scrubbed. We can see that in about 25% of the cases, a reset PPC is sufficient to recover from SEFI. In these cases, we have an actual SEFI within the PPCC (corruption of command register, program counters, stacks,…) before the FPGA is going down.

Figure 7 shows the SEFI recovery modes when DUT configuration memory is externally scrubbed. We can see that in about 40% of the cases a reset PPC is sufficient to recover from. In one occurrence, a reset DUT was sufficient to recover from a SEFI condition. With the external scrub we have almost as much SEFI within PPC than within FPGA fabric.

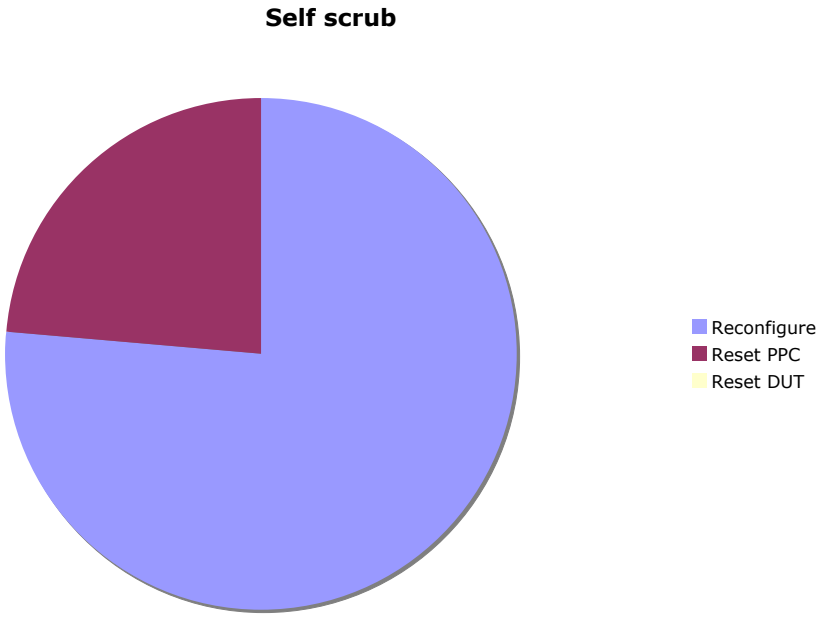

Figure 6: recoveries from SEFI when DUT configuration memory is self-scrubbed

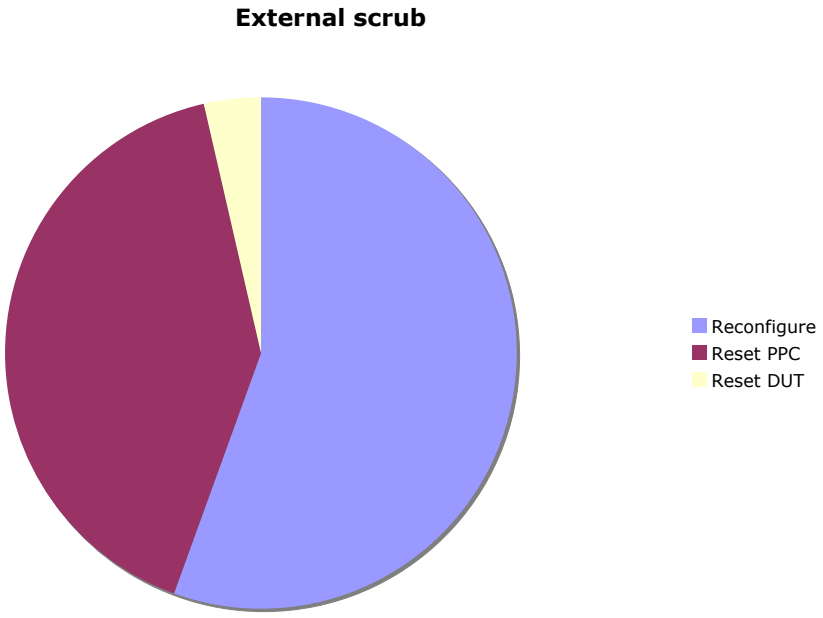

Figure 7: recoveries from SEFI when DUT configuration memory is externally scrubbed

The external scrub is a blind scrub that does not rely on any coding. It can correct any kind of error. External scrub frequency is 32 MHz. So, every configuration 32-bit word will be scrubbed every 15 ms (BRAM is not scrubbed).

Self scrub is based on a Single Error Correct Double Error Detect (SECDED) EDAC. Therefore, multiple errors within a 32 –bit word will not be corrected. Self-scrub has a frequency of 100 MHz. It is, therefore, significantly faster than external scrub. Every 32-bit word is scrubbed every 5 ms. However, when an error is detected, it takes about 100 ms to fix. Assuming a configuration memory sensitive cross-section of about 6E-07 cm^2/dev at 200 MeV, the error rates during the irradiation runs were between 1 per 5ms (flux=3E8 #/cm^2-s) and 1 per 300 ms (flux=5E+06 #/cm^2-s). As for heavy-ion, it is possible that the self-scrub was overwhelmed by the error rates for the higher fluxes. Figure 8 shows SEFI cross sections in function of protons flux for a proton energy of 200 MeV. In the case of external scrub, we can see that SEFI cross section does not change with flux except for the highest flux of 3E8 #/cm^2-s. At this flux it is clear that the external scrubber is overwhelmed, and it can be seen on SEFI cross-section. It is not so clear in the case of self-scrub.

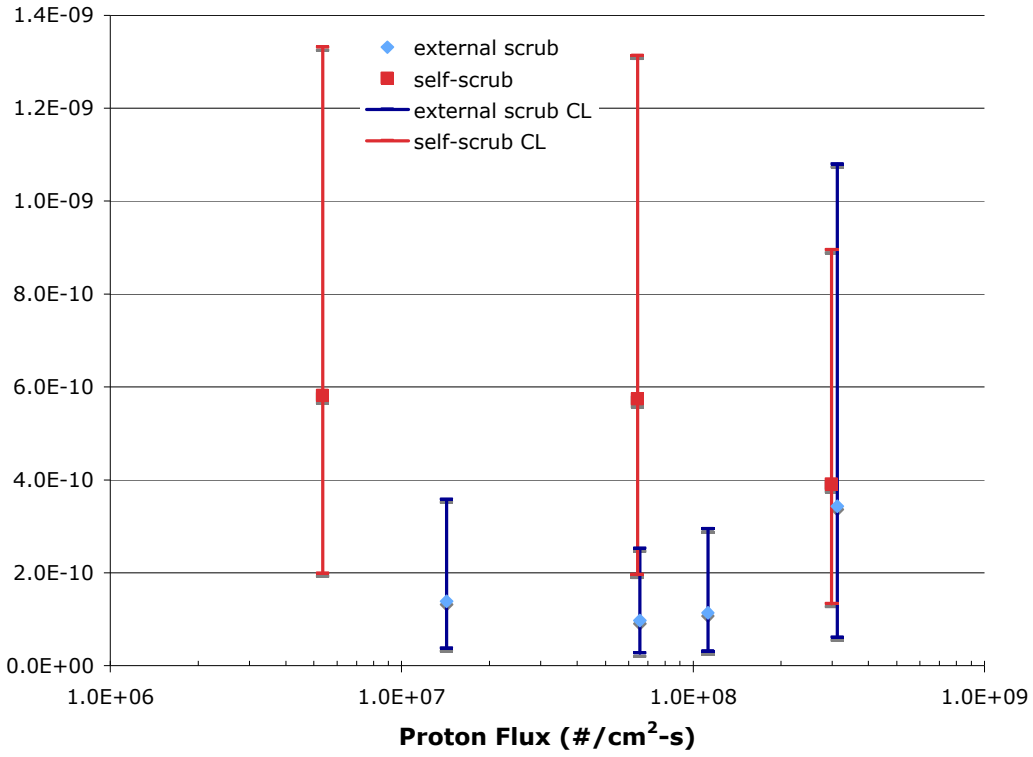

Figure 8: Effect of flux on cross-section

A SEFI in our test is defined as a timeout when one of the two PPC does not answer to interrupt requests. Other test teams[3] have reported Power On Reset (POR) SEFI and Select MAP

[3] G. Allen & al., "Initial Upset Measurements on a Virtex-4 FPGA Incorporating 90 nm Features and Thin Epitaxial Layer," presented at SEE Symposium 2007, Long Beach, CA, April 2007.

(SEFI). POR SEFI are detected if Done pin goes low, all configuration logic is reset, or if all configuration control registers are reset to preconfigures state. SMAP are detected by inability to read/write configuration memory.

Done pin went down during a handful of irradiation runs. POR SEFI cross-section is at least 2 order of magnitude than SEFI measured on this test.

As we don't perform readback during irradiation, the only way for us to see a SMAP SEFI is when we used the external scrub. A SMAP SEFI would make the scrubbing stop working. Therefore, SEFI cross-section would be higher. However, as we measure only one event per irradiation run, because of statistical fluctuations, it is very difficult to tell when a cross-section is too high. All we can say is that we never saw SEFI cross-section with external scrub that were as high as SEFI cross-section measured without scrubbing.

No high current mode was observed during these tests[3].

We also performed a few irradiation runs using PPC cache memory (without scrub only). We only observed a small, less than a factor 2, increase of SEFI cross section.

An analysis of data files showed only a very small number of data errors. We observe SEFI before we see data errors. However, out test is not data intensive. More errors are expected on a data intensive application.

After each irradiation run, we read back configuration memory via JTAG interface and stored it for further analysis. We can not use IMPACT for this analysis because it uses CRC to verify and correct. Therefore, IMPACT gives only an accurate error count for a handful of errors per frame. We sent a subset of our file to Xilinx for analysis. Results are summarized in Table 3. Table 3 gives for each test condition the average error cross sections in configuration memory per resource: routing bits, Look Up Tables (LUT), BRAM, and other miscellaneous resources. Irradiation runs with high error counts on BRAM were excluded from the analysis and the calculations of cross sections (see below for more details). Figure 11 shows a plot for 200 MeV proton energy and normal incidence.

Table 3: summary of readback files analysis

Irradiation condition	Scrub	conf/routing cross-section (cm^2/dev)	LUT cross-section (cm^2/dev)	BRAM cross-section (cm^2/dev)	Misc cross-section (cm^2/dev)
200MeV, 0 degree	no	2.36E-07	6.25E-07	1.58E-06	1.71E-08
200MeV, 0 degree	ICAP	3.05E-08	7.72E-08	1.87E-07	0.00E+00
200MeV, 0 degree	yes	2.28E-10	1.59E-08	1.67E-07	0.00E+00
200MeV, 45 degree	no	2.27E-07	4.93E-07	2.25E-06	1.84E-08
200MeV, 45 degree	ICAP	1.17E-07	5.84E-08	1.83E-07	7.02E-09
200MeV, 45 degree	yes	2.26E-09	3.87E-08	1.72E-07	1.97E-10

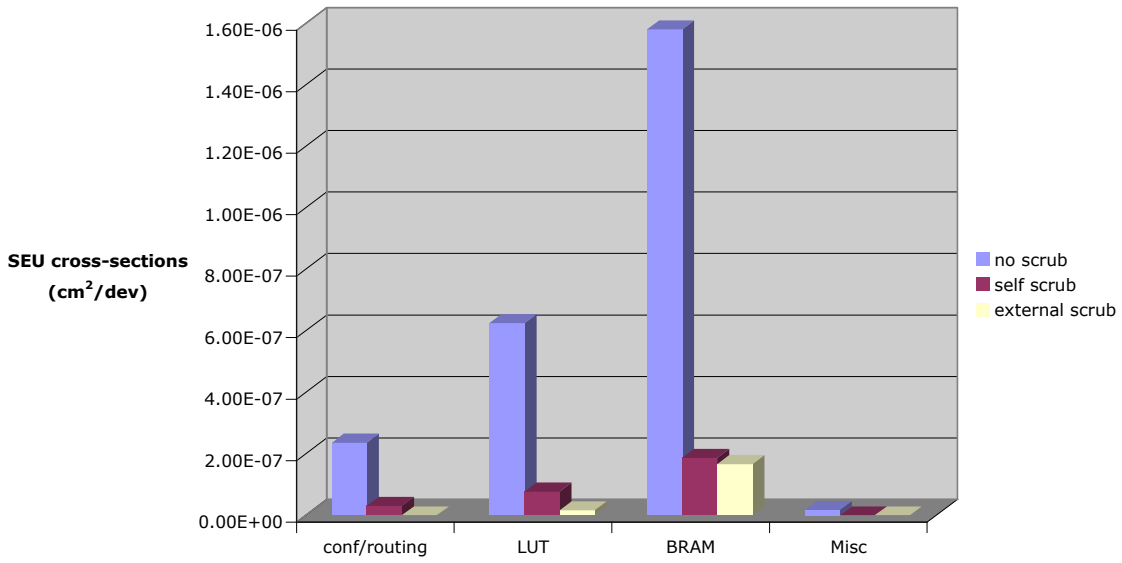

Figure 11: 200MeV irradiation, normal incidence, Error cross-sections in configuration memory per resource.

If we look at routing bits, we can see that self scrub provides a significant improvement. Theoretically the number of errors with self-scrub should be the number of uncorrectable errors or multiple bit upsets (MBU) within a 32-bit word. According to the results in Table 3 there would be about 10% of MBUs at normal incidence. It is possible that this 10% figure overestimates the percentage of MBUs as self scrub was probably overwhelmed. We can see in Table 3 the effect of angle of incidence. At 45 degrees incidence self-scrub provides only marginal improvement. This indicates a significant effect of self-scrub on the number of MBUs. With the external scrub we only have a few bits in errors. These remaining errors are due to the

nature of proton tests where not only DUT is exposed to particles. SRAM storing configuration memory in the tester board was hit, and therefore external scrub was injecting these errors. The same observation apply to the miscellaneous resources bits.

If we look at the LUT, we can see that the number of errors, and, therefore, the cross-sections are higher even though the number of LUT bits is significantly lower than the number of routing bits (about 1.55E7 routing bits for 395K LUT bits). An explanation for this is that some LUT, LUTram, are dynamic. If a design uses these LUTram, the bits will change when the circuit is exercised. This applies for SRL16 registers as well. In addition, these LUTram and SRL16 cannot be scrubbed (at least by our external blind scrub that rewrites the original state) without impairing device functionality. This is the reason why we still have some remaining differences with the initial state at configuration with the external scrub. The number of remaining errors with the external scrub is always the same and is equal to 98. We obtained the same results with heavy ions[1].

If we look at BRAM, we can see a significant difference in the number of errors for the different scrub modes, even though BRAM is not scrubbed. The reason for this is that some configuration/routing bits affect BRAM. These bits are the redundant column self-repair (256 bits), the latch mode bit (9216 bits), as well as bits controlling the width, mode, and ports. Therefore, when these configuration bits are in error, the number of errors in BRAM looks higher than he actually is. In addition, some registers that are not in configuration memory, and are therefore not scrubbable, store the redundant column address. A hit in these registers will also affect the number of BRAM errors that we see. Also, we stopped irradiation after PPC SEFI. It is possible that some of these SEFI have caused a corruption of BRAM bits. For all these reasons we have excluded from our analysis all irradiation run that presented abnormally high error counts in BRAM.

Table 4 gives bit error cross-sections for configuration bits and BRAM. Configuration bit cross-section is obtained from the number of errors in routing bit without scrubbing. BRAM bit error cross-sections are obtained from the number of errors with external scrub (without errors in routing bits) and have excluded abnormally high error counts. BRAM bits are 8T cells. They are larger than 6T cells configuration bits. Memory cells in Xilinx devices are about twice the size of typical 6T and 8T cells in similar technologies (90 nm CMOS).

Table 4: Bit error cross-sections in configuration memory

Irradiation Condition	Conf/routing cross-section (cm^2/bit)	BRAM cross-section (cm^2/bit)
200 MeV protons, normal incidence	1.52E-14	3.9E-14
200 MeV protons, 45 degrees incidence	1.46E-14	4.03E-14

VII. Summary

No destructive events were observed during protons tests. However, XC4VFX60 Xilinx FPGA is very sensitive to proton induced SEE. Without scrubbing of configuration memory SEFI sensitivity is high. Self scrub performs better with protons than it performed with heavy ions, at least at normal incidence. However, the effect on SEFI cross-section is small. External scrub provides a significant improvement with a factor 10 reduction in SEFI cross-section.

In one occurrence out of about 100 irradiation runs, it was necessary to power cycle DUT to recover from SEFI condition. We don't know enough to attribute this the DUT itself or a hit to the tester board or JTAG/USB interface.